## REMARKS

In the January 28, 2008 Office Action, all of the claims stand rejected in view of prior art. No other objections or rejections were made in the Office Action.

### *Status of Claims and Amendments*

In response to the January 28, 2008 Office Action, Applicant has amended claims 1-4, cancelled claims 5-7 and introduced new claims 8-10, as indicated above. Thus, claims 1-4 and 8-10 are pending, with claims 1, 8 and 10 being the only independent claims. Reexamination and reconsideration of the pending claims are respectfully requested in view of above amendments and the following comments.

### *Rejections - 35 U.S.C. § 103*

In paragraph 2 of the Office Action, claims 1-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,781,599 (Shiga) in view of U.S. Patent No. 6,300,985 (Lowe). In response, Applicant has amended independent claim 1 and cancelled claims 5-7, as mentioned above.

More specifically, independent claim 1 now clearly recite a data conversion system in which one of a plurality of nodes on an IEEE1394 bus serves as a cycle master, transmits data from one of the plurality of nodes to another node of the plurality of nodes in synchronism with a cycle start packet output from the cycle master, and converts the data in the other node of the plurality of nodes, wherein ***a first node of the plurality of nodes comprises*** an external synchronizing signal receiver for receiving an external reference signal provided on at least one of the first and second nodes, and a synchronization adjustment unit for synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal received by the external synchronizing signal receiver, and ***the first node or***

***a second node of the plurality of nodes comprises a data conversion unit for converting the data and outputting the converted data in synchronism with the reference signal.***

Clearly this arrangement is ***not*** disclosed or suggested by the Shiga patent, the Lowe patent or any other prior art of record.

Applicant strongly disagrees with the characterization in the Office Action of the Shiga patent. Specifically, page 3 of the Office Action states that:

> Shiga also discloses, a synchronization adjustment unit (cycle timer, Shiga column 4, lines 36-39) for synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal received by the external synchronizing signal receiver (the cycle timer utilizes the sync time included periodically within incoming packets to adjust for the lag between the source and the receiver, Shiga column 4, lines 40-47).

This is not what the Shiga patent says. Rather, from the Shiga patent states that

> the sync time is defined as a time which is indicated by a cycle timer of the P1394 serial bus when the DBN is equal to zero. The cycle timer is provided in each piece of equipment, and it has a time which cycles at a predetermined rate (128 seconds, for example).
>
> The clock signals at the transmission side and the reception side are independent of each other, and are not synchronous with each other, so that an error between the clock signals is accumulated and a time lag is gradually increased between the write-in rate of the bit stream into the FIFO at the transmission side and the read-out rate of the bit stream from the FIFO at the reception side. The sync time is used as information to adjust this time lag. (Shiga, column 4 lines 36-47)

Further, the Shiga patent discloses "a synchronizing packet representing the start time of the communication cycle (cycle start packet)" (see Column 1, lines 34-37), as well as disclosing an isochronous data packet and an asynchronous data packet. From the Shiga Patent

disclosure and in particular Fig. 6, it can be understood that the cycle start packet, the isochronous data packet and the asynchronous data packet are separate and distinct.

In the Shiga patent it also states that ". . . transmitted with an isochronous data packet on the P1394 serial bus" (Shiga column 3, lines 50-51), it can be understood that the "packets" that are subsequently used means the isochronous data packet. In addition, the description of "there are two groups of packets, each packet of one group being provided with a sync time (Sync Time) while each packet of the other group is provided with no sync time" (Shiga column 4, lines 29-32) means that the packet provided with Sync Time is transmitted as the isochronous data packet on the P1394 serial bus. The isochronous transmission has constant frequency of cycle timer in Shiga. Therefore, the teachings of the Shiga patent are different from the specific configuration required by amended independent claim 1. Specifically the Shiga patent fails to disclose ***synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal received by the external synchronizing signal receiver*** as required by amended independent claim 1.

It is well settled in U.S. patent law that the mere fact that the prior art can be modified does ***not*** make the modification obvious, unless a reason exists for making the modification. Neither the Shiga patent nor the Lowe patent considered alone or in combination with one another disclose the combination of features required in independent claim 1.

Moreover, Applicant believes that the dependent claims 2-4 are also allowable over the prior art of record in that they depend from independent claim 1, and therefore are allowable for the reasons stated above. Also, the dependent claims 2-4 are further allowable because they include additional limitations. Thus, Applicant believes that since the prior art of record does not disclose or suggest the invention as set forth in independent claim 1, the

prior art of record also fails to disclose or suggest the inventions as set forth in the dependent claims.

Therefore, Applicant respectfully requests that this rejection be withdrawn in view of the above comments and amendments.

*New Claims*

Applicant has added new claims 8-10 by the current Amendment. Applicant believes that new claims 8-10 further distinguish the invention over the cited prior art. Independent claim 8 recites a device for transmitting a cycle start packet serving as a cycle master on an IEEE1394 bus and converting data transmitted from a node connected on the IEEE1394 bus in synchronism with the cycle start packet that includes an external synchronizing signal receiver for receiving a reference signal. Claim 8 goes on to require that the device further includes a data conversion unit for converting the data and outputting the converted data in synchronism with the reference signal and a synchronization adjustment unit for synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal.

The configuration required by new independent claim 8 is neither disclosed nor suggested by the cited prior art.

Independent claim 10 recites a device for generating a cycle start packet serving as a cycle master on an IEEE1394 and transmitting data to a node connected on the IEEE1394 bus in synchronism with the cycle start packet that includes an external synchronizing signal receiver for receiving a reference signal. Claim 10 further requires a synchronization adjustment unit for synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal.

The configuration required by new independent claim 10 is neither disclosed nor suggested by the cited prior art.

***Prior Art Citation***

In the Office Action, additional prior art references were made of record. Applicant believes that these references do not render the claimed invention obvious.

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In view of the foregoing amendment and comments, Applicant respectfully asserts that claims 1-4 and 8-10 are now in condition for allowance. Reexamination and reconsideration of the pending claims are respectfully requested.

Respectfully submitted,

/John C. Robbins/
John C. Robbins
Reg. No. 34,706

GLOBAL IP COUNSELORS, LLP
1233 Twentieth Street, NW, Suite 700
Washington, DC 20036
(202)-293-0444
Dated: June 24, 2008

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